What is claimed is:

1. A flash type analog to digital converting method, comprising:

(a) receiving an analog signal and generating a 2^n-bit digital thermometer code based on the analog signal;

(b) compressing the 2^n-bit thermometer code to generate a digital signal having compressed thermometer code; and

(c) encoding the the compressed thermometer code to generate an n-bit digital signal.

2. The method of claim 1, wherein in the step (b) the 2^n-bit thermometer code is compressed j times to generate a $(2^{n-j}+j)$-bit thermometer code, where $j \geq 1$.

3. The method of claim 2, wherein in the step (b) the 2^n-bit thermometer code is compressed to a 2^{n-j}-bit digital signal by folding the 2^n-bit thermometer code j times and XORing corresponding bits of the thermometer code with one other, and j-number of carries are generated by generating a $(2^{n-j-1}+1)_{th}$-bit digital signal having the 2^n-bit thermometer code as a carry.

4. A flash type analog to digital converting method, comprising:

(a) receiving an analog signal and generating a a 128-bit digital thermometer code based on the analog signal;

(b) 3_{rd}-compressing the 128-bit thermometer code to generate a 16-bit thermometer code and a 3-bit carry; and

(c) encoding the the 128-bit of thermometer code to generate a 7-bit digital signal.

5. The method of claim 4, wherein the step (b) includes:

a 1_{st}-compression step of generating a 64-bit thermometer code by folding the 128-bit thermometer code and XORing the corresponding bits of the 128-bit thermometer code with one another and generating a 65_{th}-bit of the 128-bit thermometer code as a first carry;

a 2_{nd}-compression step of generating a 32-bit thermometer code by folding the 64-bit thermometer code and XORing the corresponding bits of the 64-bit thermometer code with one another and generating a 33_{rd} bit of the 64-bit thermometer code as a second carry; and

a 3_{rd}-compression step of generating a 16-bit thermometer code by folding the 32-bit thermometer code and XORing the corresponding bits of the 32-bit thermometer code with one another and generating a 17_{th} bit of the 32-bit of thermometer code as a third carry.

6. A flash type analog to digital converting circuit, comprising:

a thermometer code generating means for receiving an analog signal and generating a 2^n-bit digital thermometer code based on the analog signal;

a thermometer code compression means for compressing the 2^n-bit thermometer code to generate a compressed thermometer code; and

an encoding means for encoding the compressed thermometer code to generate an n-bit digital signal.

7. The circuit of claim 6, wherein the thermometer compression means compresses the 2^n-bit thermometer code j times to generate a $(2^{n-j}+j)$-bit thermometer code, where $j \geq 1$.

8. The circuit of claim 7, wherein the thermometer compression means compresses the 2^n-bit thermometer code to a 2^{n-j}-bit digital signal by folding the 2^n-bit thermometer code j times and XORing corresponding bits of the thermometer code with one another and generating j-number of carries by generating a $(2^{n-j-1}+1)_{th}$-bit digital signal having the 2^n-bit thermometer code as a carry.

9. A flash type analog to digital converting circuit, comprising:

a thermometer code generating means for receiving an analog signal and generating a 128-bit digital thermometer code based on the analog signal;

a thermometer code compression means for 3_{rd}-compressing the 128-bit thermometer code to generate a 16-bit thermometer code and a 3-bit carry; and

an encoding means for encoding the 128-bit thermometer code to generate a 7-bit digital signal.

10. The circuit of claim 9, wherein the thermometer code compression means includes:

a 1_{st}-compression means for generating a 64-bit thermometer code by folding the 128-bit thermometer code and XORing the corresponding bits of the 128-bit thermometer code with one another and generating a 65_{th} bit of the 128-bit thermometer code as a first carry;

a 2_{nd}-compression means for generating a 32-bit thermometer code by folding the 64-bit thermometer code and XORing the corresponding bits of the 64-bit thermometer code with one another and generating a 33_{rd} bit of the 64-bit thermometer code as a second carry; and

a 3_{rd}-compression means for generating a 16-bit thermometer code by folding the 32-bit thermometer code and XORing the corresponding bits of the 32-bit thermometer code with one another and generating a 17_{th} bit of the 32-bit thermometer code as a third carry.

11. A flash type analog to digital converting circuit, comprising:

a thermometer code generating circuit that receives an analog signal and generates a 2^n-bit thermometer code based on the analog signal;

a thermometer code compression circuit that compresses the 2^n-bit thermometer code to generate a compressed thermometer code; and

an encoder that encodes the compressed thermometer code to generate an n-bit digital signal.

12. The circuit of claim 11, wherein the thermometer compression means compresses the 2^n-bit thermometer code j times to generate a $(2^{n-j}+j)$-bit thermometer code, where $j \geq 1$.

13. The circuit of claim 12, wherein the thermometer compression circuit compresses the 2^n-bit thermometer code to a 2^{n-j}-bit digital signal by folding the 2^n-bit thermometer code j times and XORing corresponding bits of the 2^n-bit thermometer code with one another and generating j-number of carries by generating a $(2^{n-j-1}+1)_{th}$-bit digital signal having the 2^n-bit thermometer code as a carry.